Network-on-Chip Architectures: A Holistic Design Exploration: 45 (Lecture Notes in Electrical Engineering)

Chrysostomos Nicopoulos, Vijaykrishnan Narayanan, Chita R. Das

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[2]. The Cell Processor from Sony, Toshiba and IBM (STI) [3], and the Sun UltraSPARC T1 (formerly codenamed Niagara) [4] signal the growing popularity of such systems. Furthermore, Intel's very recently announced 80-core TeraFLOP chip [5] exemplifies the irreversible march toward many-core systems with tens or even hundreds of processing elements. 1.2 The Dawn of the Communication-Centric Revolution The multi-core thrust has ushered the gradual displacement of the computati- centric design model by a more communication-centric approach [6]. The large, sophisticated monolithic modules are giving way to several smaller, simpler p- cessing elements working in tandem. This trend has led to a surge in the popularity of multi-core systems, which typically manifest themselves in two distinct incarnations: heterogeneous Multi-Processor Systems-on-Chip (MPSoC) and homogeneous Chip Multi-Processors (CMP). The SoC philosophy revolves around the technique of Platform-Based Design (PBD) [7], which advocates the reuse of Intellectual Property (IP) cores in flexible design templates that can be customized accordingly to satisfy the demands of particular implementations. The appeal of such a modular approach lies in the substantially reduced Time-To- Market (TTM) incubation period, which is a direct outcome of lower circuit complexity and reduced design effort. The whole system can now be viewed as a diverse collection of pre-existing IP components integrated on a single die.

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